

FIG. 1

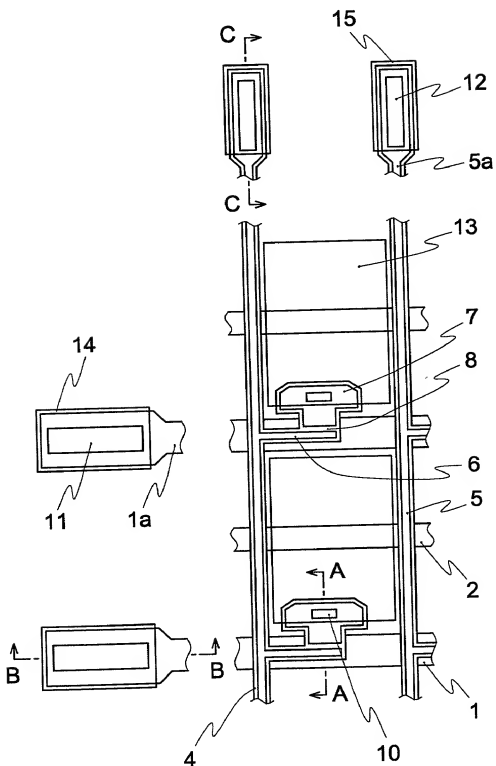


FIG. 2(a)

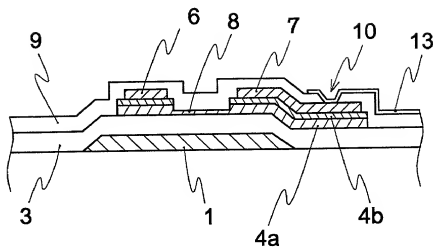


FIG. 2(b)

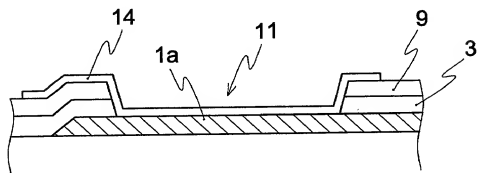


FIG. 2(c)

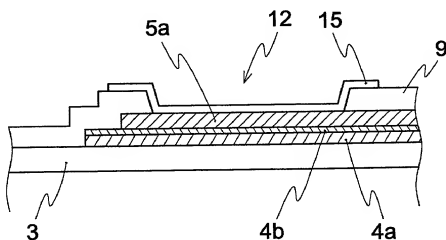


FIG. 2(d)

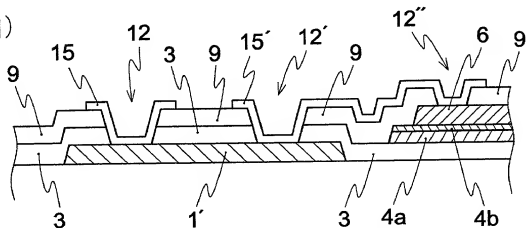


FIG. 3

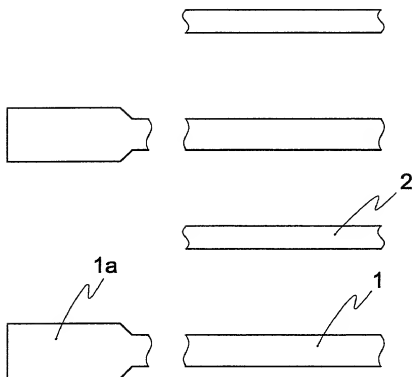


FIG. 4

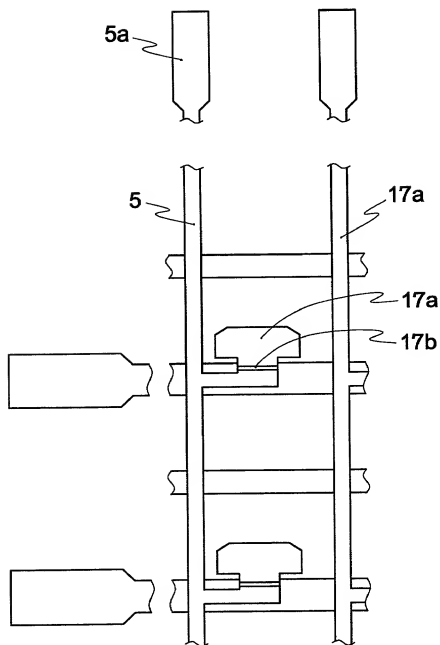


FIG. 5

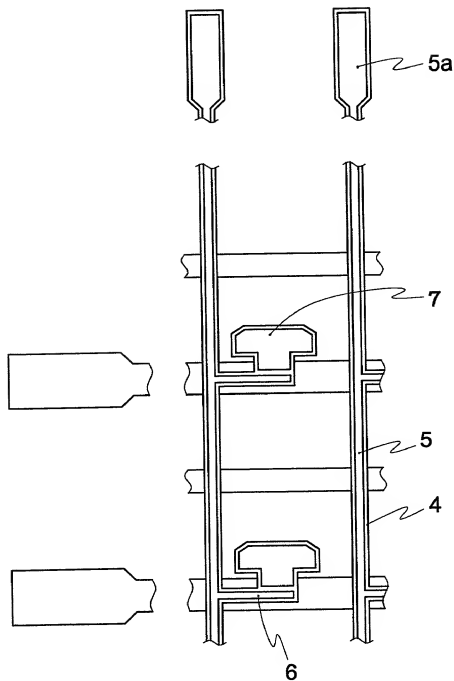


FIG. 6

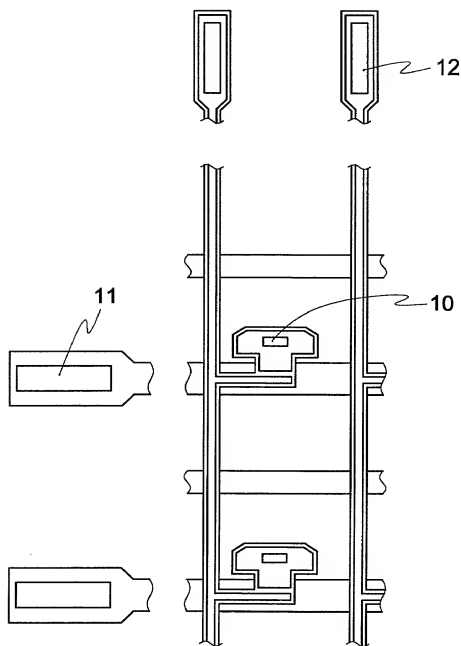


FIG. 7

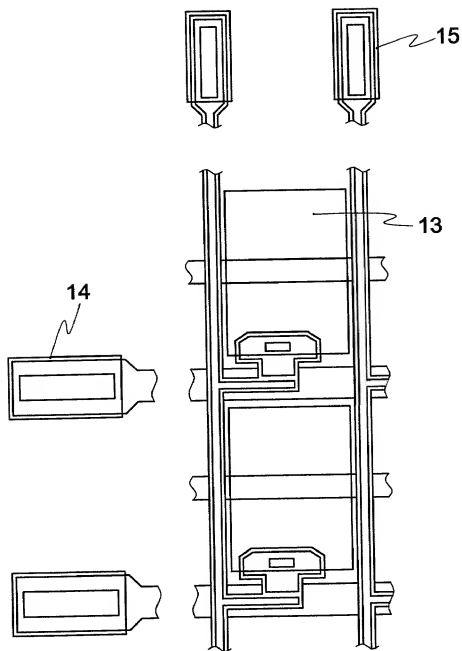


FIG. 8

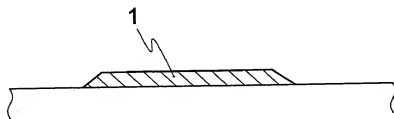


FIG. 9

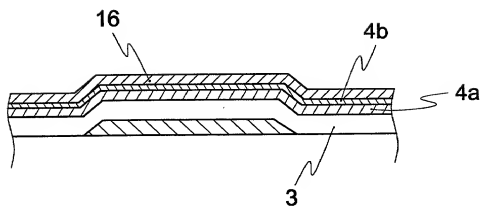


FIG. 10

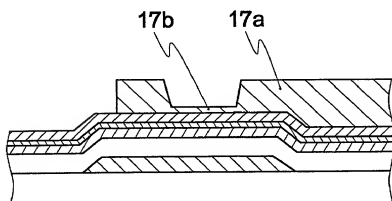


FIG. 11

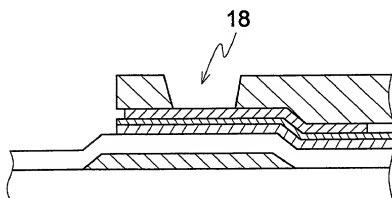




FIG. 12

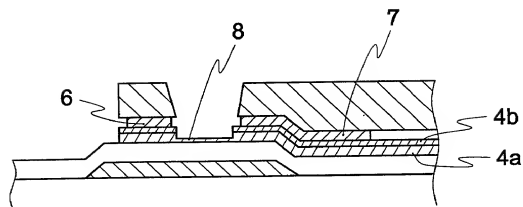


FIG. 13

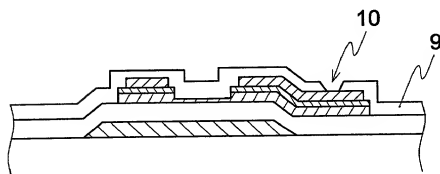


FIG. 14

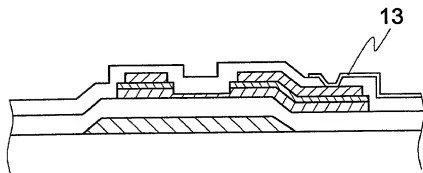


FIG. 15

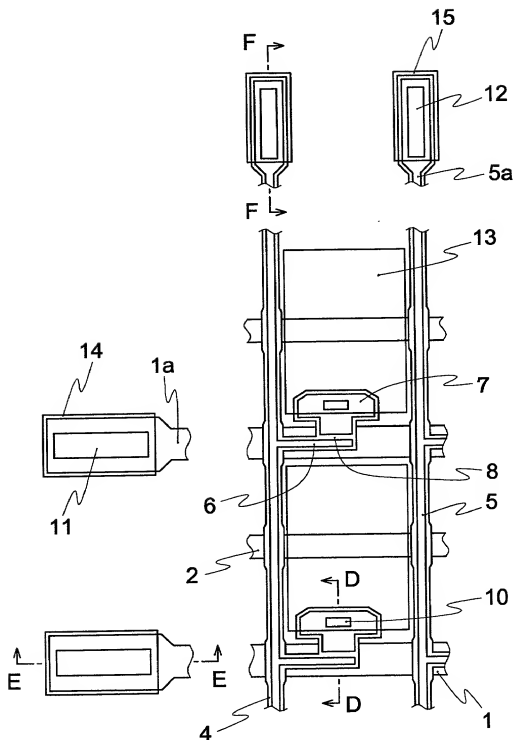


FIG. 16

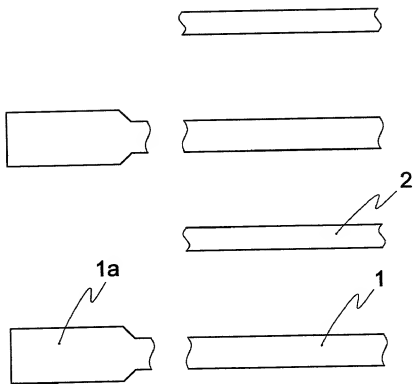


FIG. 17

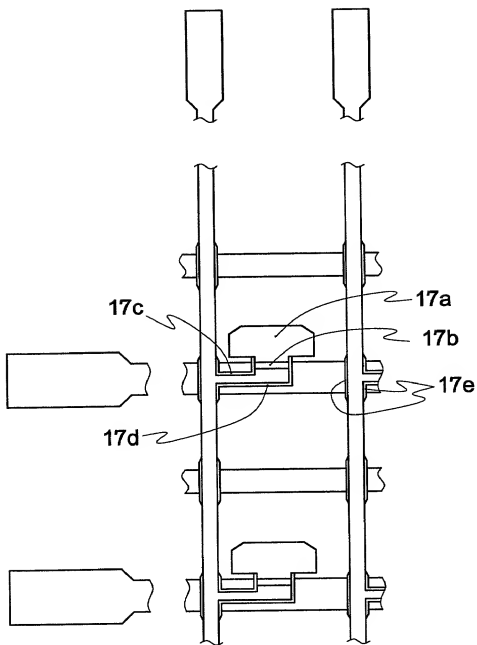


FIG. 18

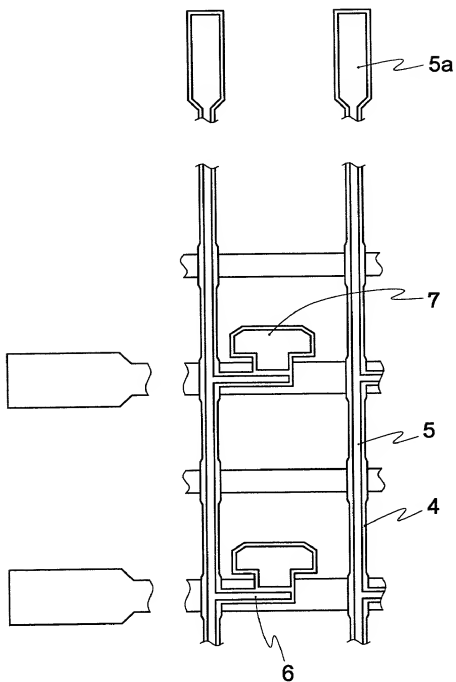


FIG. 19

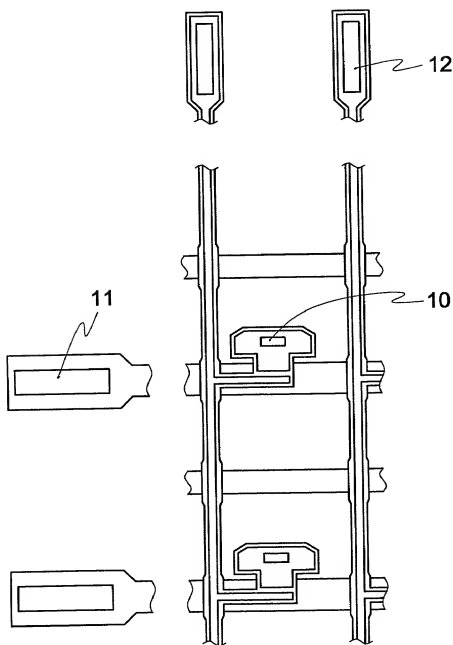


FIG. 20

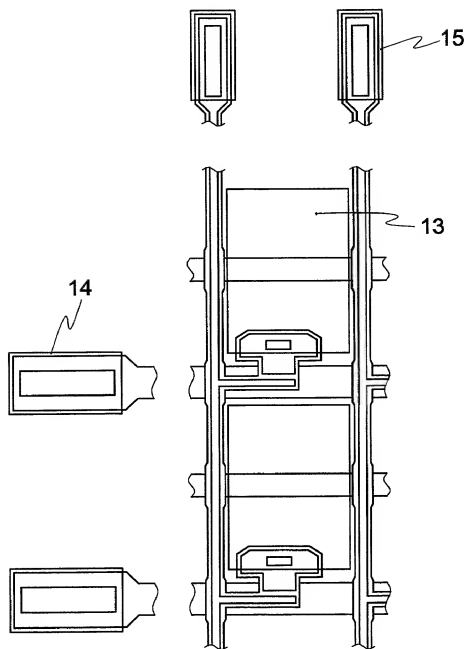


FIG. 21

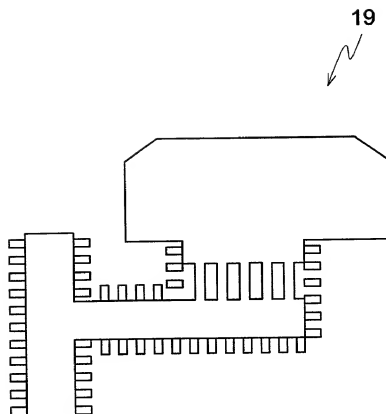




FIG. 22

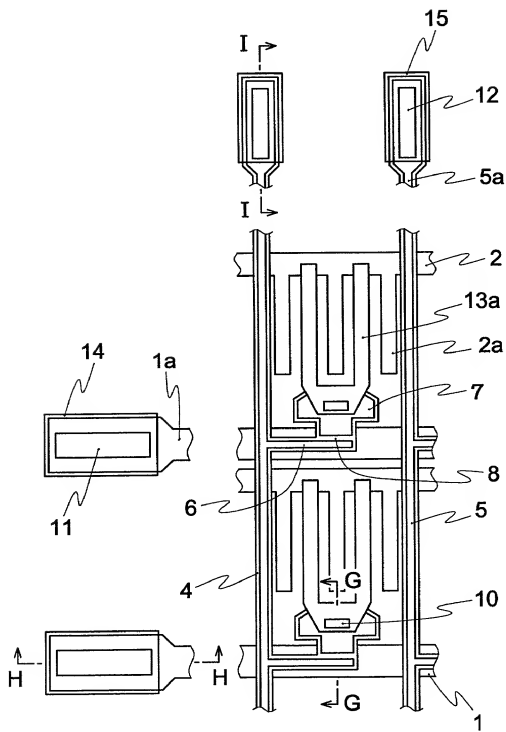


FIG. 23

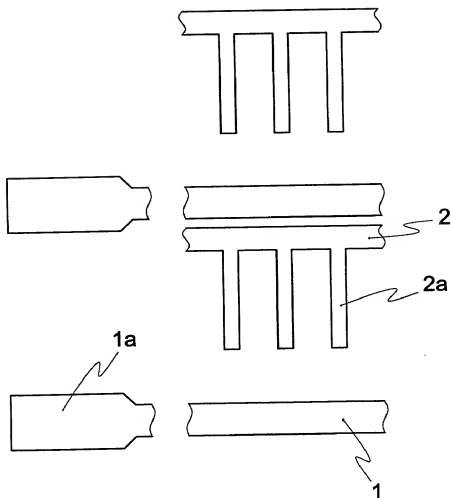


FIG. 24

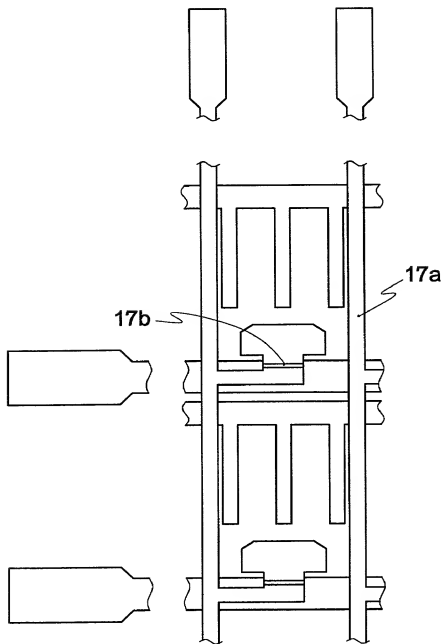


FIG. 25

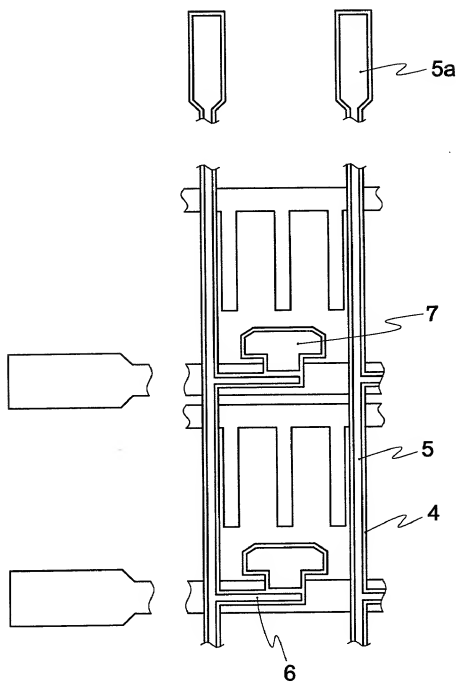


FIG. 26

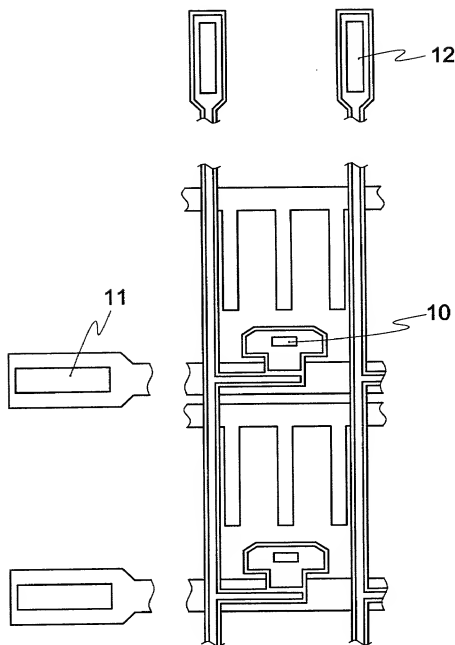


FIG. 27

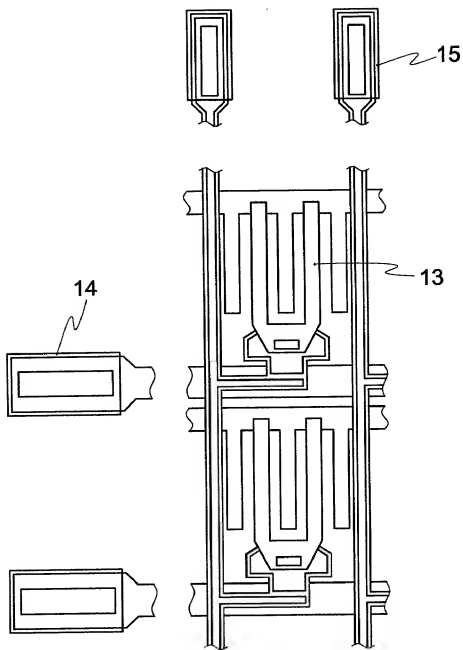


FIG. 28

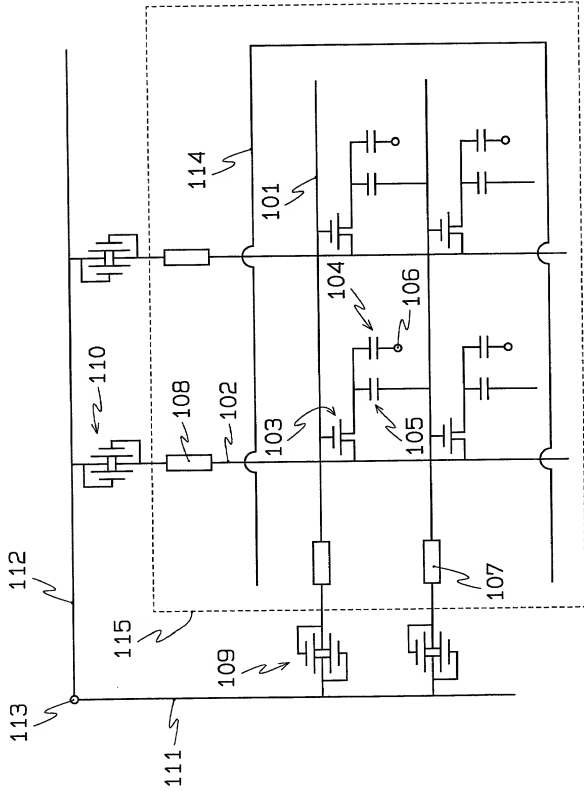


FIG. 29(a)

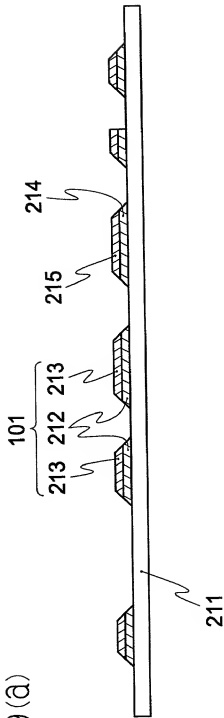


FIG. 29(b)

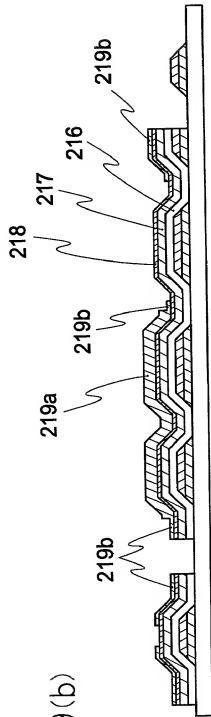




FIG. 30(a)

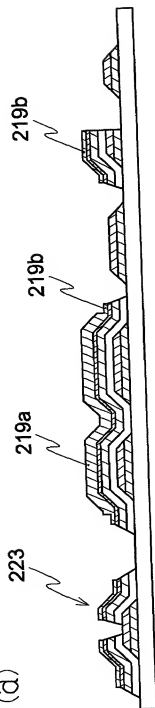


FIG. 30(b)

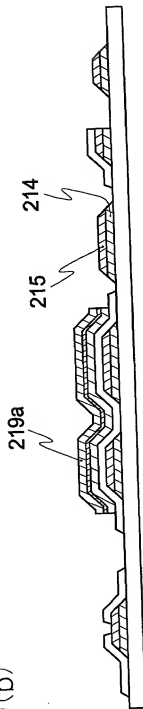


FIG. 31(a)

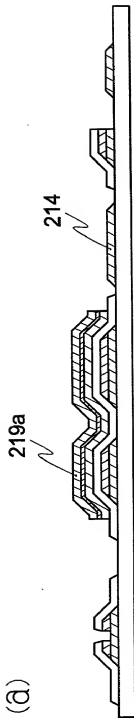


FIG. 31(b)

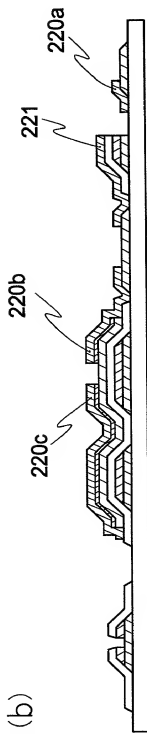


FIG. 31(c)

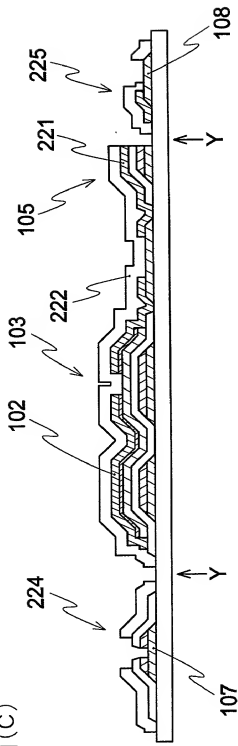


FIG. 32(a)

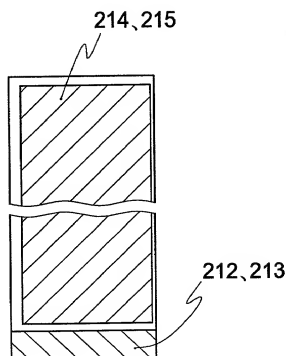


FIG. 32(b)

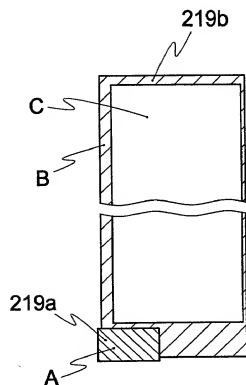


FIG. 32(c)

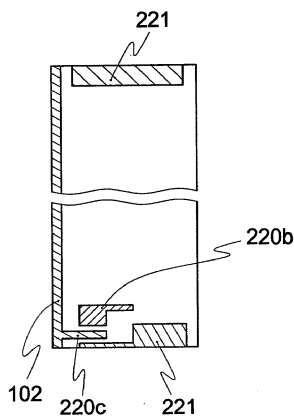


FIG. 32(d)

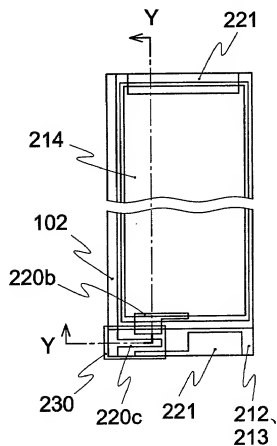


FIG. 33

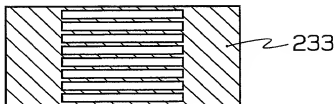


FIG. 34

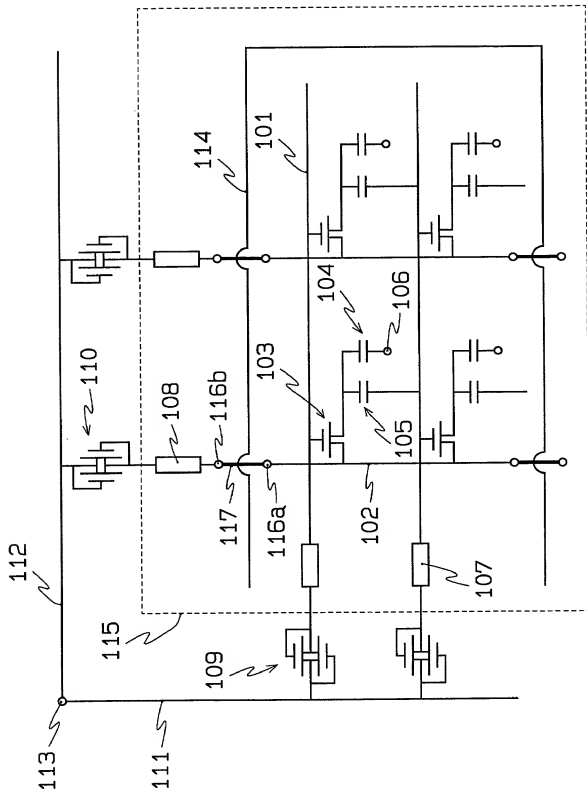


FIG. 35

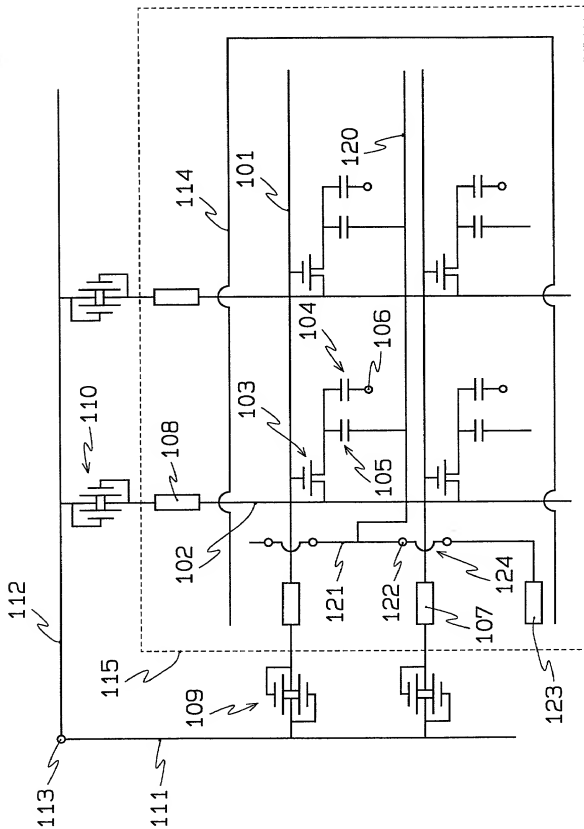


FIG. 36

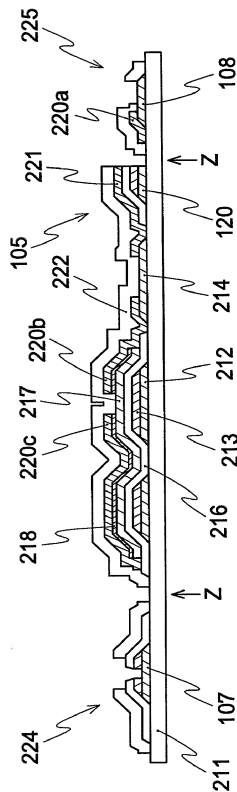


FIG. 37(a)

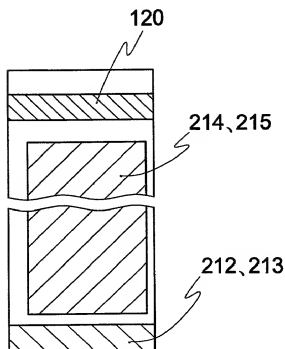


FIG. 37(b)

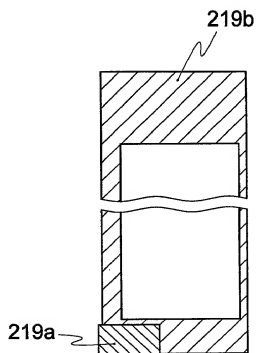


FIG. 37(c)

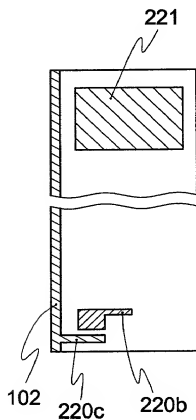


FIG. 37(d)

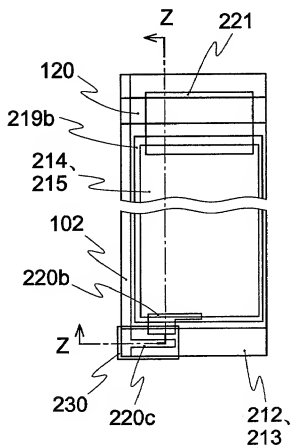




FIG. 38

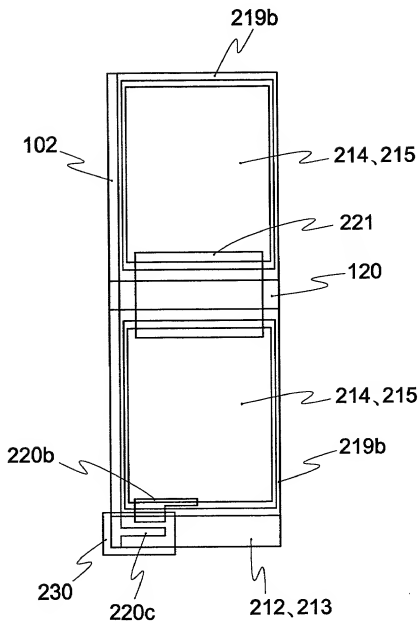


FIG. 39

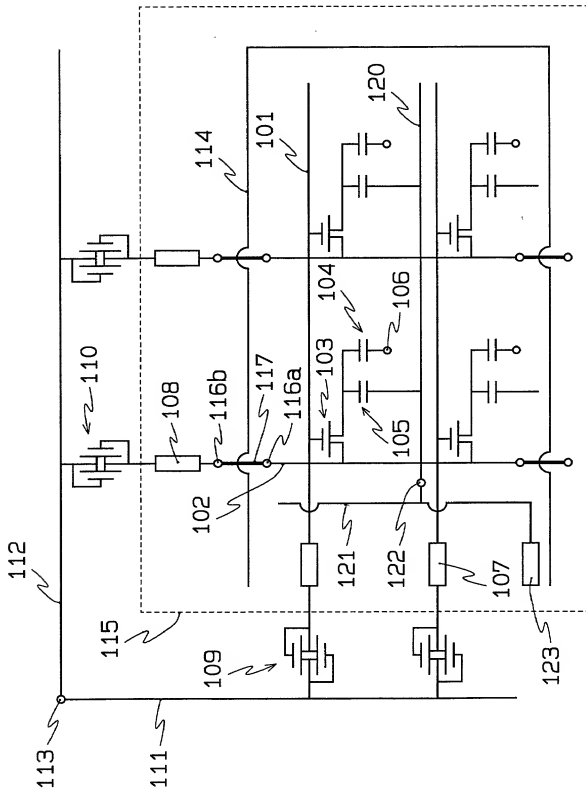


FIG. 40

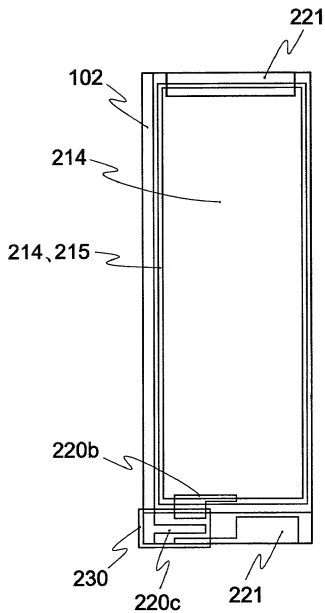


FIG. 41(a)

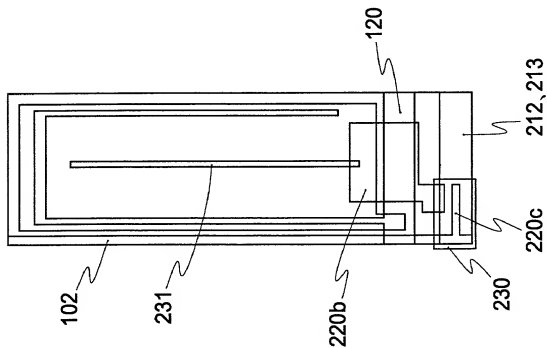


FIG. 41(b)

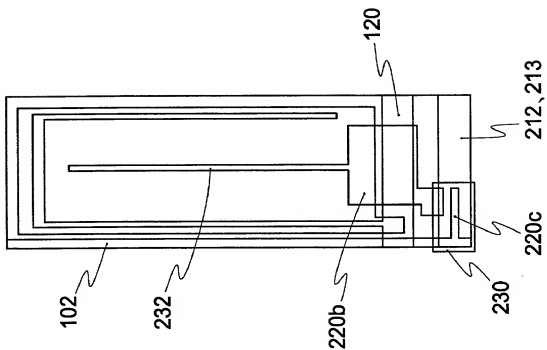


FIG. 42(a)

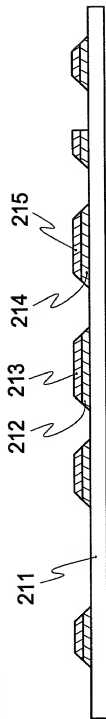


FIG. 42(b)

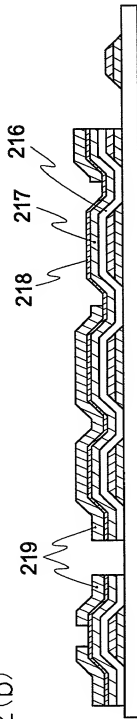


FIG. 42(c)

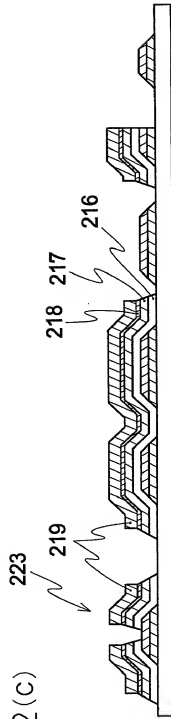


FIG. 43(a)

FIG. 43(a)

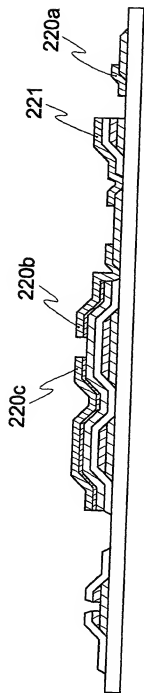


FIG. 43(b)

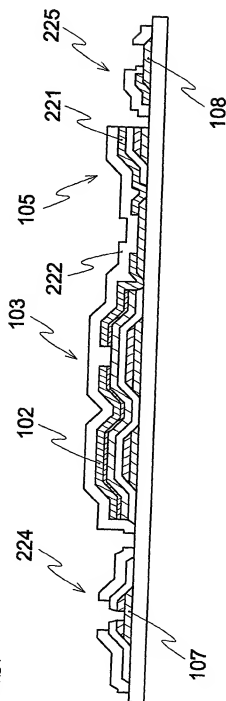


FIG. 44(a)

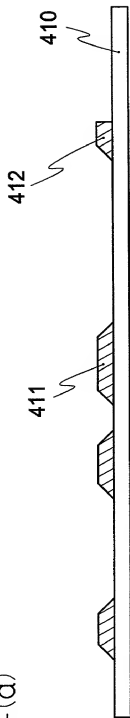


FIG. 44(b)

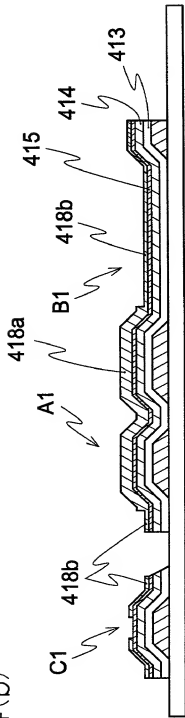


FIG. 44(c)

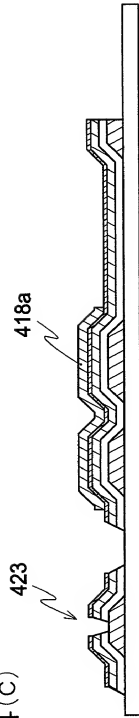


FIG. 45(a)

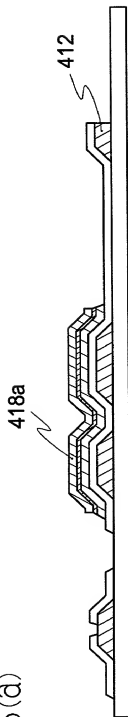


FIG. 45(b)

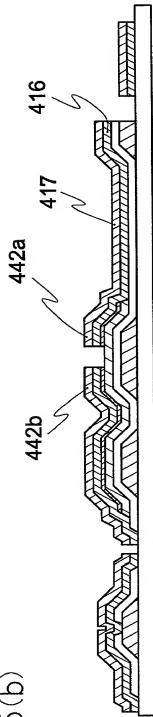


FIG. 45(c)

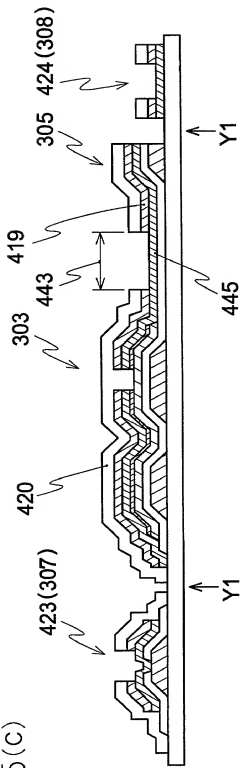




FIG. 46(a)

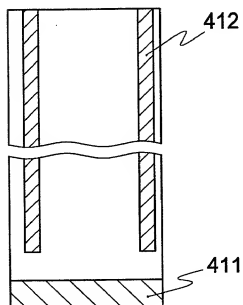


FIG. 46(b)

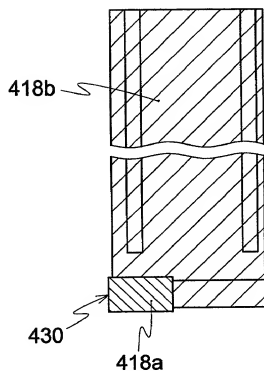


FIG. 46(c)

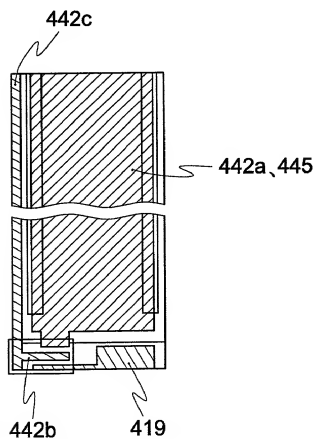


FIG. 47(a)

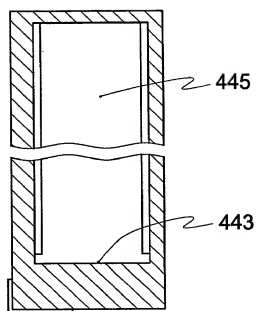


FIG. 47(b)

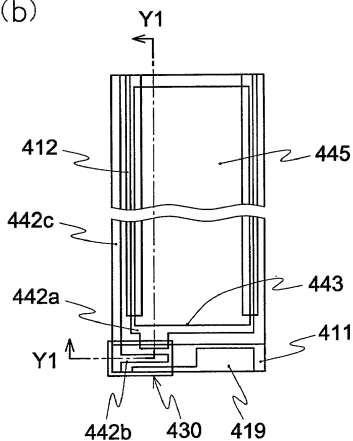


FIG. 48

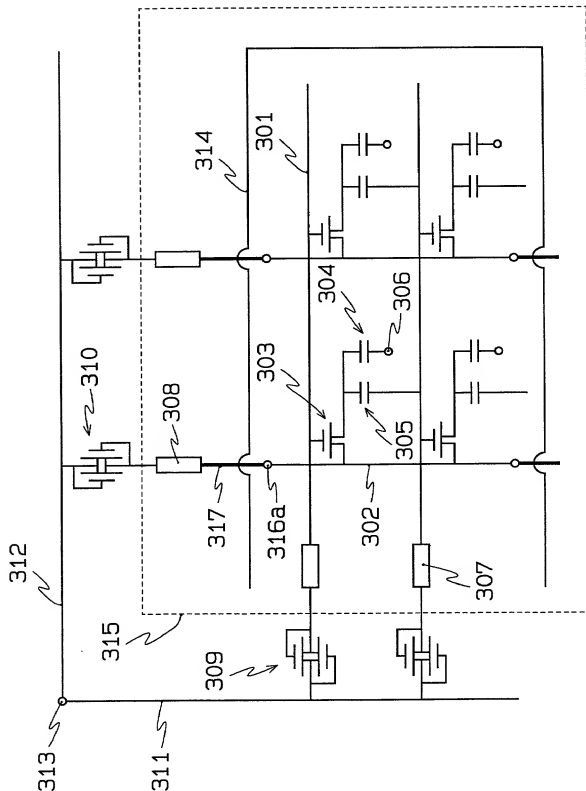


FIG. 49

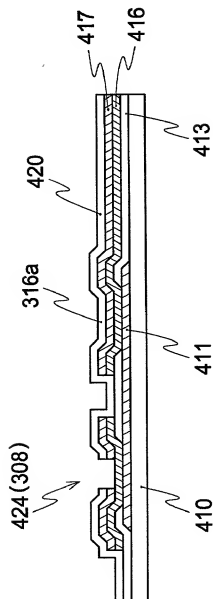


FIG. 50

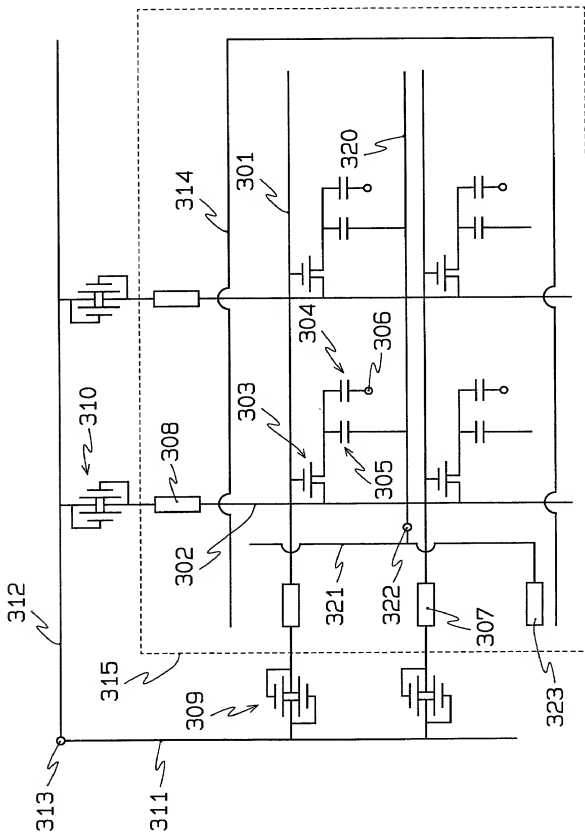


FIG. 51

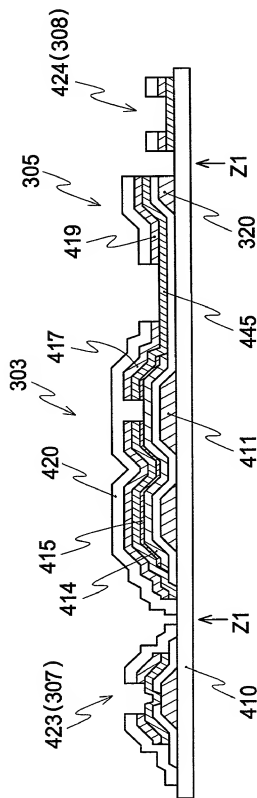


FIG. 52(a)

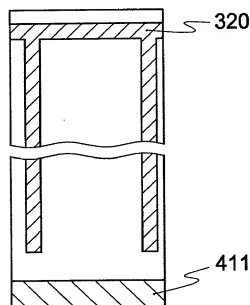


FIG. 52(b)

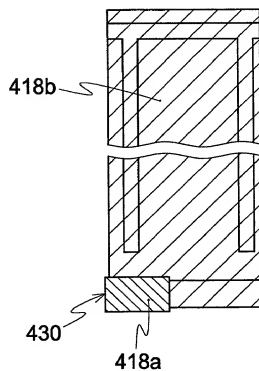


FIG. 52(c)

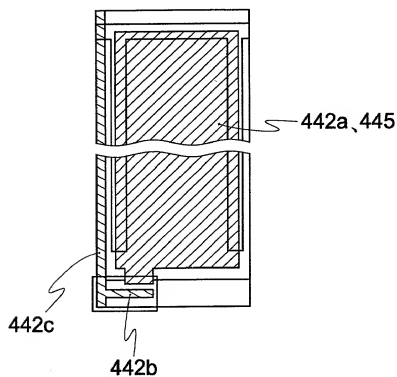


FIG. 53(a)

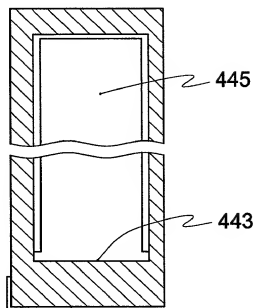
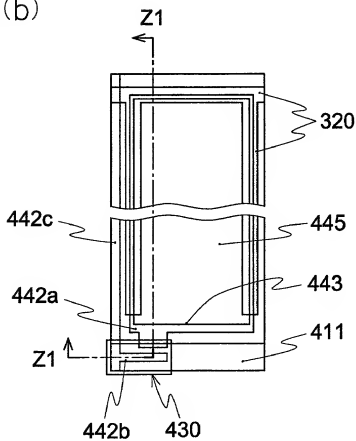


FIG. 53(b)





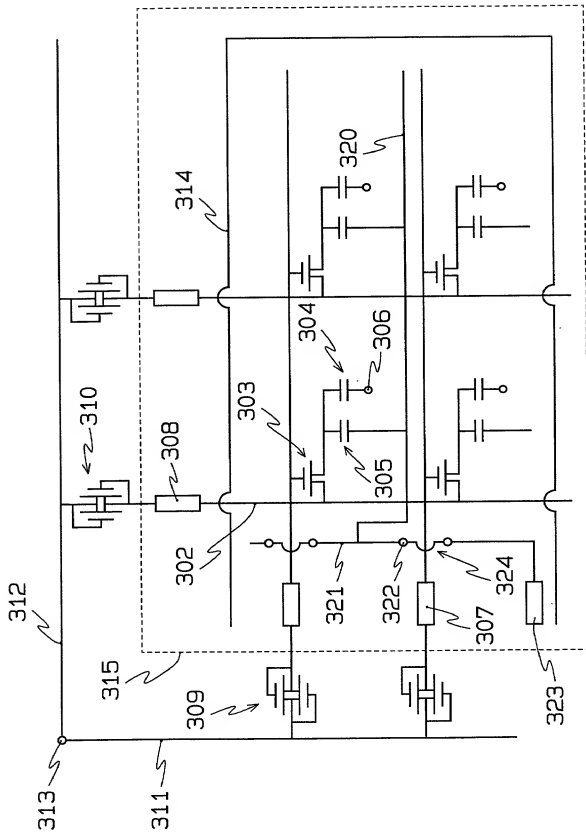
[illegible]

FIG. 55

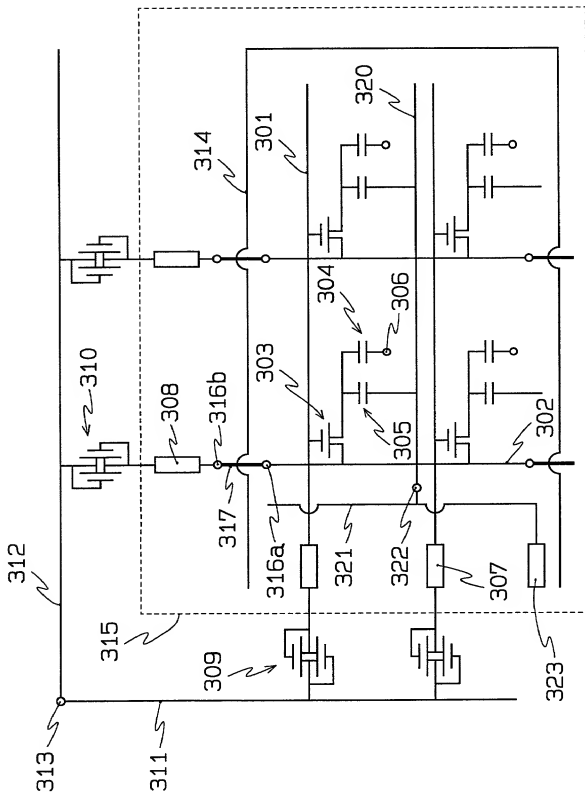
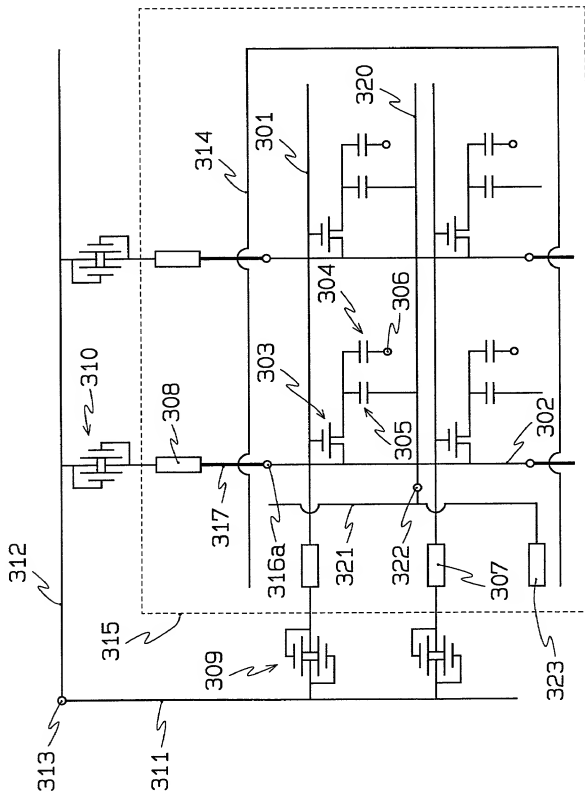


FIG. 56



This cross-sectional view shows a semiconductor device with a substrate 51. A gate stack 52 is formed on the substrate, featuring a gate dielectric 53 and a gate electrode 54. The gate stack is patterned into a series of gates 55, 56, 57, 58, and 59. A conductive layer 60 is deposited on top of the gate stack and is patterned into a series of contacts 61. The contacts 61 are electrically connected to the gate electrodes 54 through the conductive layer 60.

FIG. 58

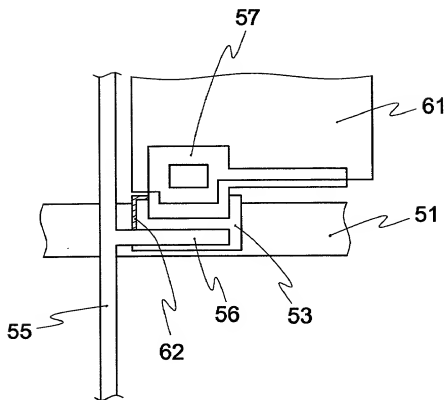


FIG. 59(a)



FIG. 59(b)

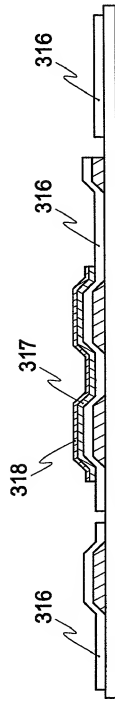


FIG. 59(c)

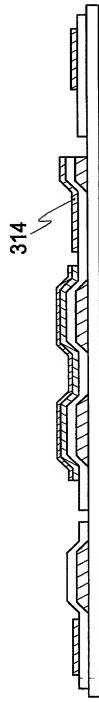


FIG. 60(a)

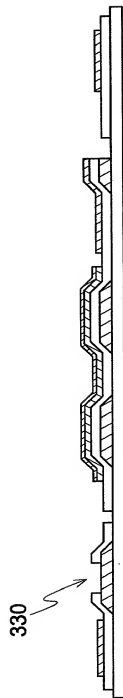


FIG. 60(b)

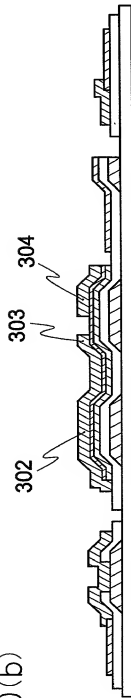


FIG. 60(c)

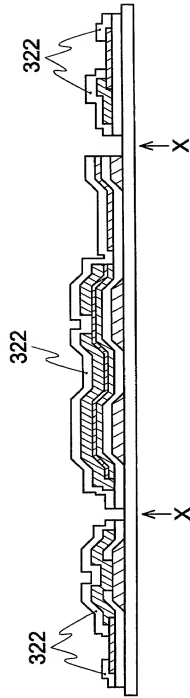


FIG. 61(a)

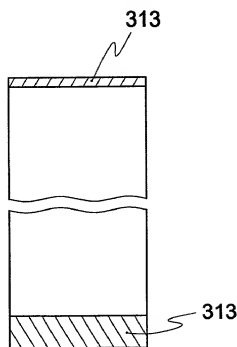


FIG. 61(b)

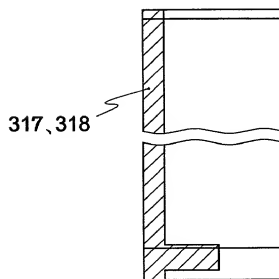


FIG. 61(c)

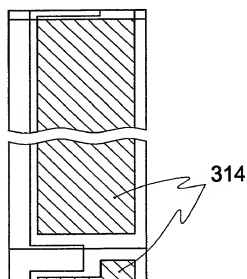


FIG. 61(d)

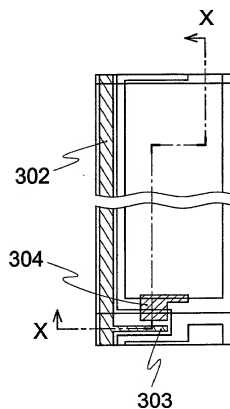




FIG. 62(a)

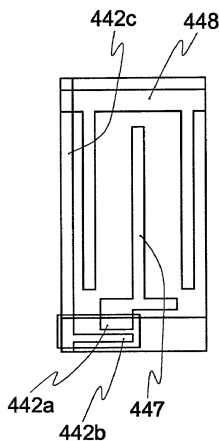


FIG. 62(b)

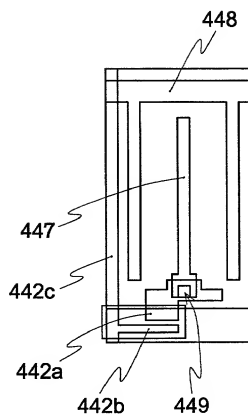


FIG. 62(c)

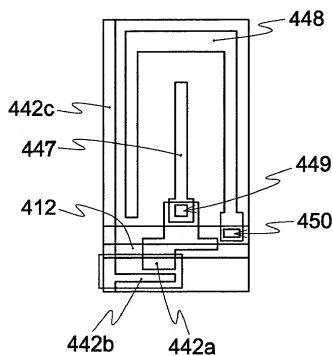


FIG. 63(a)

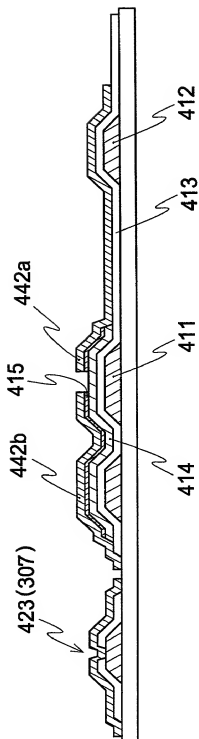
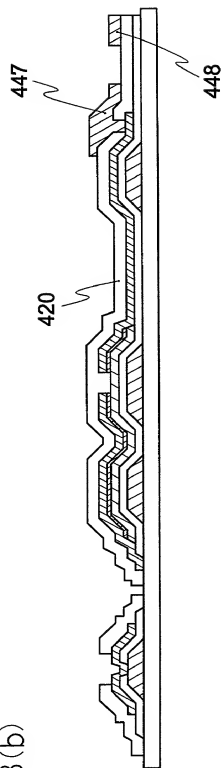


FIG. 63(b)



4

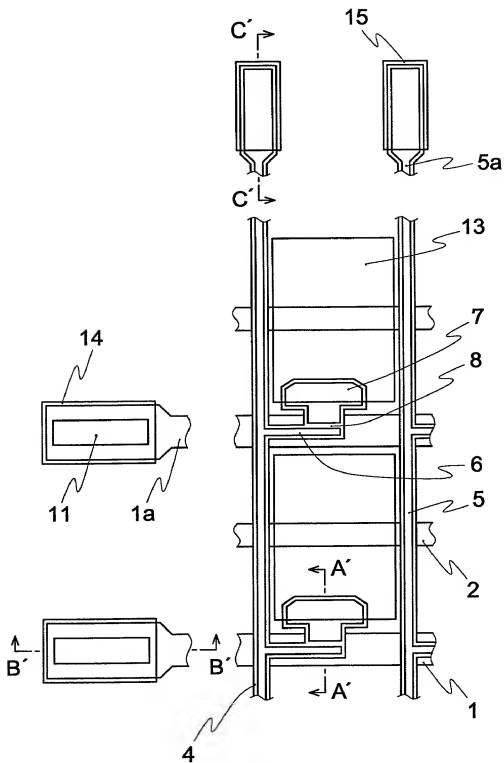


FIG. 65(a)

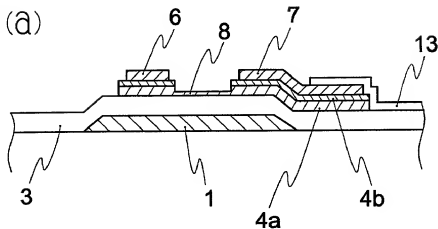


FIG. 65(b)

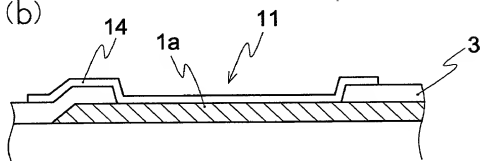


FIG. 65(c)

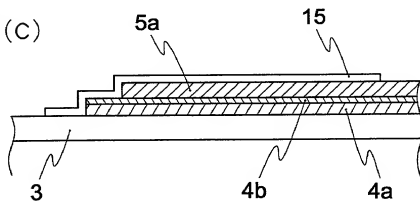


FIG. 65(d)

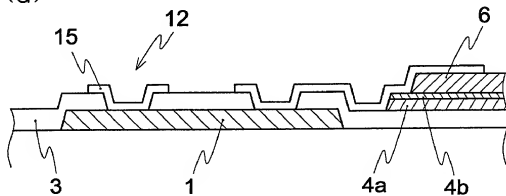


FIG. 66

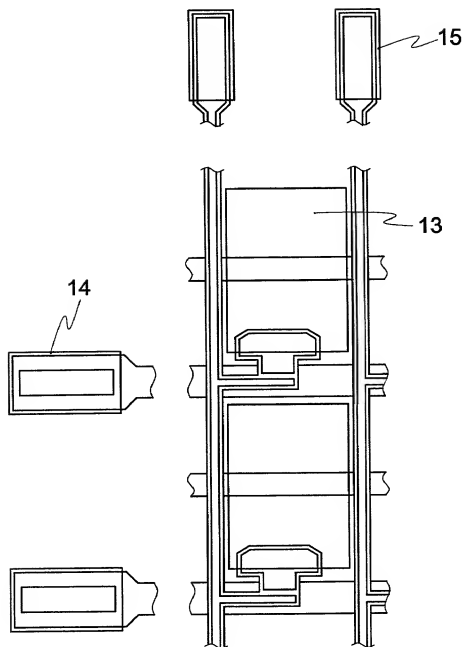


FIG. 67

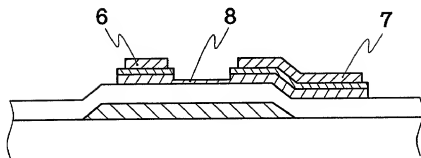


FIG. 68

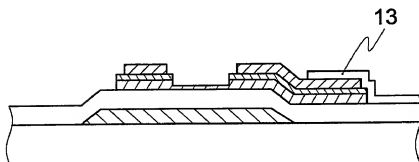


FIG. 69

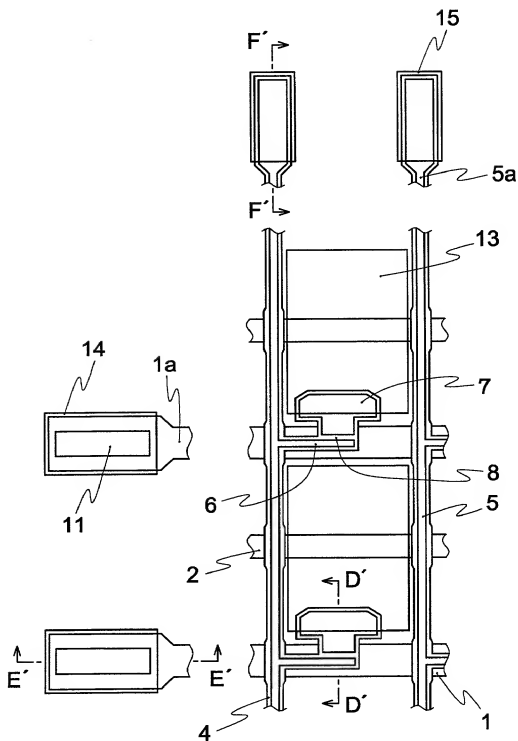


FIG. 70

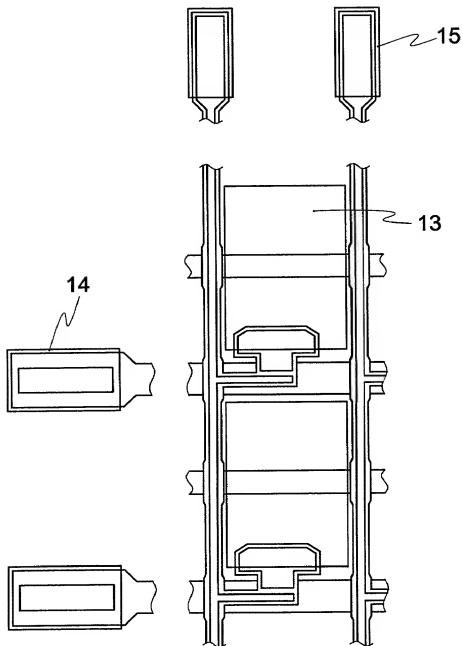




FIG. 71

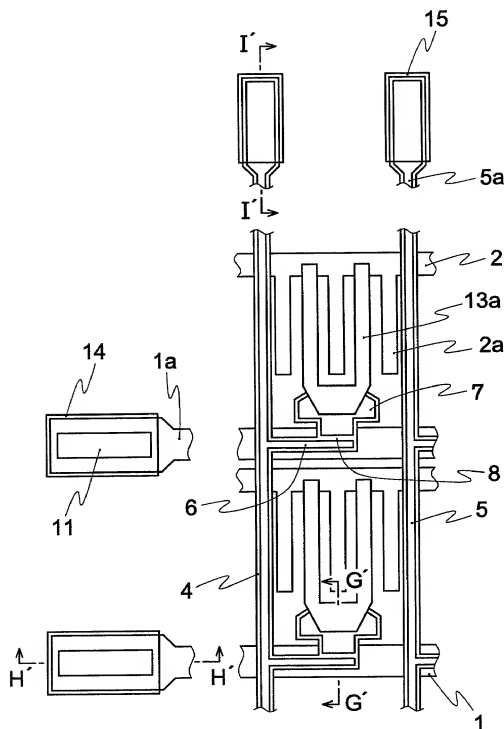


FIG. 72

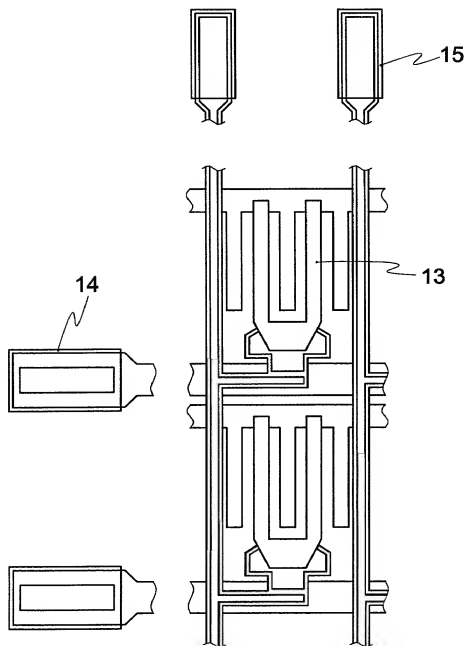


FIG. 73

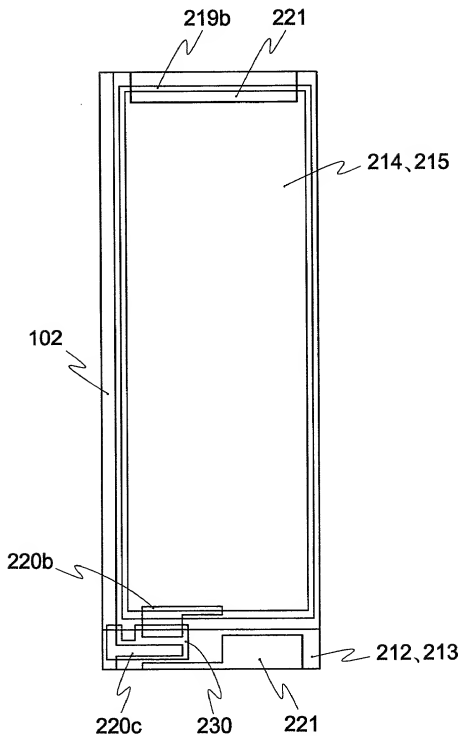


FIG. 74

